

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions and listings of claims in the application:

**LISTING OF CLAIMS:**

1. (currently amended): An electrical signal regenerator comprising:  
an equalizer;  
a clock data recovery circuit; and  
a switch,

wherein said switch being is operable to either connect the data recovery circuit to the an output of the equalizer when an input signal of a higher bitrate multiplex signal is input to the switch is detected, or to bypass the data recovery circuit and connect to the output of the equalizer to the output when an input signal of a lower bitrate multiplex signal is detected input to the switch.

2. (original): An electrical signal regenerator according to claim 1, wherein the clock data recovery circuit comprises a detector for detecting the bitrate of the input signal.

3. (currently amended): An electrical signal regenerator according to claim 1 comprising a delimiter decision circuit for deciding upon logical signal value 0 or 1.

**AMENDMENT UNDER 37 C.F.R. § 1.111**  
**U.S. Patent Application No.: 10/753,327**  
**Attorney Docket No.: Q78982**

4. (original): An electrical signal regenerator according to claim 1, comprising a test loop controllably connectable from the output to the input of the regenerator.

5. (original): An electrical signal regenerator according to claim 1, wherein said equalizer being an analogue equalizer comprising a tapped delay line.

6. (currently amended): An electrical signal regenerator according to claim 1, wherein said equalizer being an analogue equalizer comprising a first tap and a second tap, the first tap having a higher delay than the second tap, both taps being connected to a adder-subtractor for generating a difference-signal corresponding to a difference between output signals of the first and second taps.

7. (currently amended): An electrical signal regenerator according to claim 6, wherein the signal ratio-ratio between the two taps is adjustable.

8. (currently amended): An electrical signal regenerator according to claim 6, wherein the signal ratio-ratio between the two taps is adjustable, and wherein the ratio-ratio is determined by two peak detectors.

9. (currently amended): A network element, comprising internal electrical signal paths, wherein at least part of said paths are terminated by an electrical signal regenerator comprising

| an equalizer and a clock data recovery circuit and a switch, said switch being operable to either  
| connect the data recovery circuit to an output when an input signal of a higher bitrate multiplex  
| signal is detected or to bypass the data recovery circuit and connect the equalizer to the output  
| when an input signal of a lower bitrate multiplex signal is detected.

10. (original): A network element according to claim 9 being an optical crossconnect comprising an electrical space switching matrix, said matrix comprising a number of switch modules being interconnected by means of internal electrical cables, an electrical signal regenerator is coupled to one end of each internal electrical cable in front of a switching module.

11. (currently amended): A network element according to claim 10, wherein said ~~matrix switching~~ modules being adapted to output a test signal at each unused output port and wherein the electrical signal regenerators ~~are is~~ adapted to raise an alarm when neither a test signal nor a valid input signal is detected.

12. (original): A method of transmitting an electrical signal having either a first or a second bitrate, wherein the first bitrate is higher than the second bitrate, said method comprising the steps of

transmitting said electrical signal via a signal path;

detecting the bitrate of said electrical signal received from the signal path;

in the case the electrical signal has the first bitrate, performing a first regeneration of said electrical signal and then performing a second regeneration and

in the case the signal has the second bitrate, performing said first regeneration of said signal, only.

13. (original): A method according to claim 12, wherein said first signal regeneration is an electrical equalization and wherein said second signal regeneration is a clock data recovery.

13. (new): An electrical signal regenerator according to claim 4, wherein a static test signal is fed via the test loop to an input of the equalizer while no external signal is input to the input of the equalizer.

14. (new): An electrical signal regenerator according to claim 8, wherein a first detector of the two peak detector is connected to an input of the equalizer to detect a static test input signal, and a second detector of the two peak detector is connected to an output of the first tap.

15. (new): An electrical signal regenerator according to claim 1, wherein the higher bit rate is approximately 10 Gbit/s and the lower bit rate is approximately 2.7 Gbits/s.